1974

AN-729
Application Note

A MEDIUM COST PLL VARACTOR TUNING SYSTEM UTILIZING OFF-THE-SHELF LOGIC

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A unique frequency domain tuning scheme for varactor TV tuners. The purpose of a frequency domain tuning system is to control a TV varactor tuner complement so that the proper local oscillator frequency is obtained for the channel number selected.

MOTOROLA *Semiconductor Products Inc.*

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INTRODUCTION

A varactor TV tuner is one step in the direction of a more reliable TV tuner. While it solves the mechanical RF switch contact problem, it creates dc stability and tuner address problems. Various analog touch tuning systems have evolved to solve the tuner address problem, but the impetuous dc stability problem remains. A solution to this problem is to address the tuner in the frequency domain. These frequency domain techniques are usually very complex, requiring custom logic to make them reasonable in terms of the number of circuit logic blocks, but in turn, are even more expensive. The objective of this design was to utilize off-the-shelf parts in the medium price range (as low as possible) to obtain the most cost-effective frequency domain varactor tuning address system devised to date.

HOW IT WORKS

The heart of this system is a frequency comparator which compares a processed sample of the tuner local oscillator to a reference frequency. When the comparator detects a difference in its two input frequencies, an error signal is sent to the tuning voltage generator which in turn controls the tuning voltage sent to the varactor tuners, so that a frequency match is obtained. In other words, it operates like a typical phase-locked loop (PLL) system. The unique feature about this system is the processing of the local oscillator sample. The frequency allocations for the TV channels do not follow any single pattern. In the typical PLL system, this would require custom logic to obtain the proper divide by N numbers for each of the 82 channels. Also, reasonable dividers are not available for the UHF local oscillator frequency range of 517 through 931 MHz. To solve these problems, the local oscillator samples are offset by mixing so that the resultant frequency for each channel is equal to N times 6 MHz; where N is uniquely the channel number, i.e., the channel 2 processed local oscillator frequency is 12 MHz, and the channel 83 processed local oscillator frequency is 498 MHz.

SYSTEM OPERATION

Figure 1 shows the basic block diagram of the PLL tuning system. The input to the system by the user is by means of a ten-button keyboard (0-9). To select a channel, he must press a button for the tens digit, and then press a button for the units digit. This enters the channel number selected into the memory latch which addresses the seven-segment readout, provides the divide by N counter with N, and keys the B+ control circuitry so that the proper circuits are enabled. The tuners are switched into the proper band by the B+ control circuitry and a sample of the active tuner local oscillator is fed through the appropriate oscillator offset circuitry. The oscillator sample frequency is then offset the proper amount in the mixer by the appropriate offset oscillator which was also turned on by the B+ control circuitry. This offset oscillator sample is then amplified and filtered and fed to the divider. The divider then divides the offset local oscillator sample by 50 and then divides by N which was obtained from the memory. The output of the divider goes to the comparator, where it is compared to the reference frequency.

When a frequency match is not obtained, the comparator sends an error signal to the tuning voltage generator, such that, the tuning voltage is "ramped" in the direction to produce a frequency match at the comparator.

The following sections give the details of each of the building blocks.

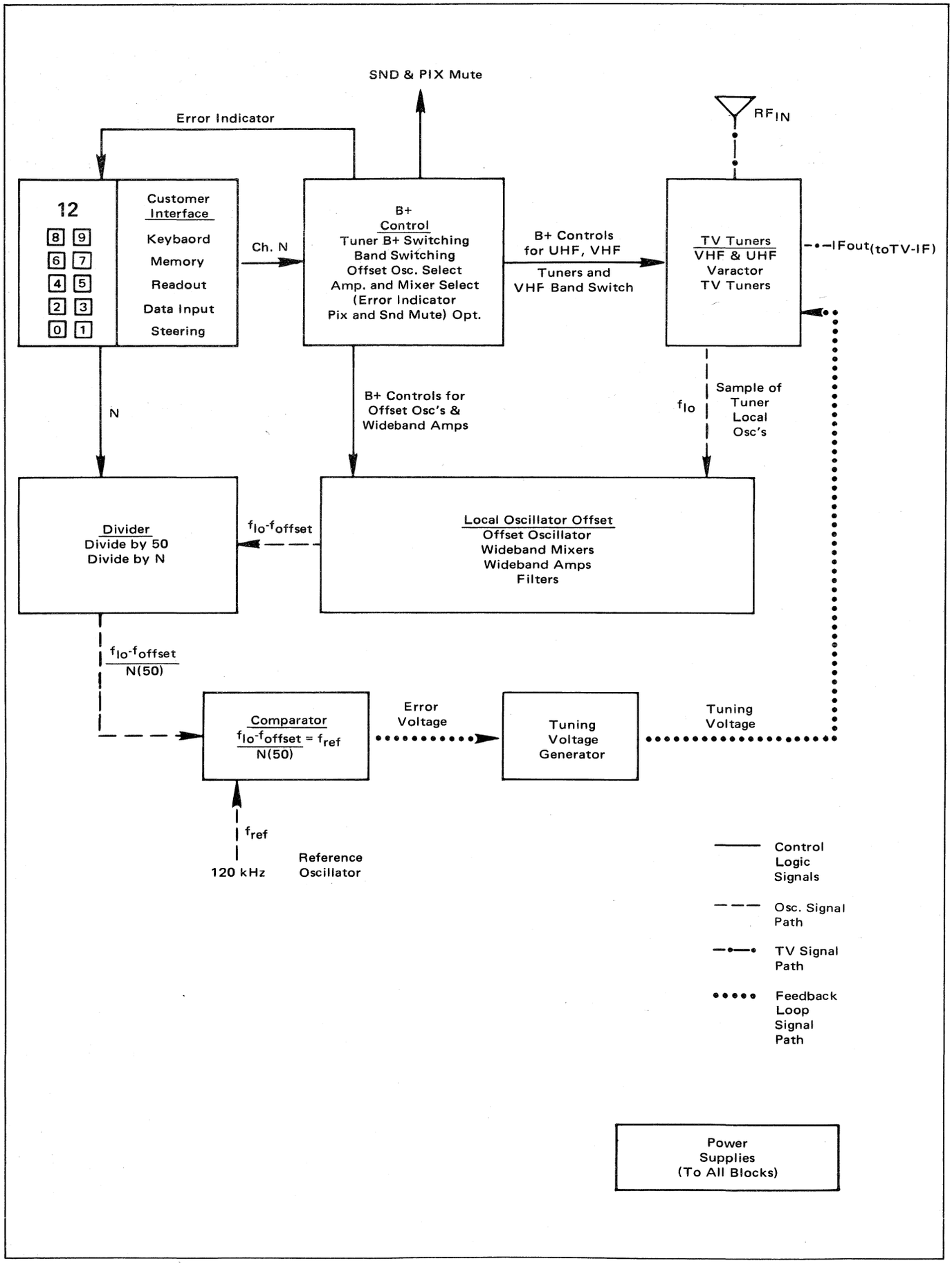


FIGURE 1 – PLL Tuning System Basic Block Diagram

OFFSET OSCILLATORS

The local oscillator (L.O.) offset circuits are divided up into two sections, VHF shown in Figure 2, and UHF shown in Figure 3. They were designed to perform the following three major functions:

1. Offset the UHF local oscillator frequency range to a maximum of 500 MHz so that reasonably priced off-the-shelf dividers can be used.
2. Establish a relationship between channel numbers and the associated tuner local oscillator frequency for that channel in a way such that the divide by N counter can divide by channel number. This eliminates the need for a pre-programmed random access memory.
3. Offset the VHF and UHF tuner local oscillator in a manner that evens out the gaps between the bands and channels to some constant so that the phase-locked loop system can be made as simple as possible.

To perform these functions, the TV broadcast channels were divided into four groups at the points where the tuner local oscillator frequency exceeded 6 MHz between stations. To determine the proper offset oscillator frequency for each of the groups and establish a relationship

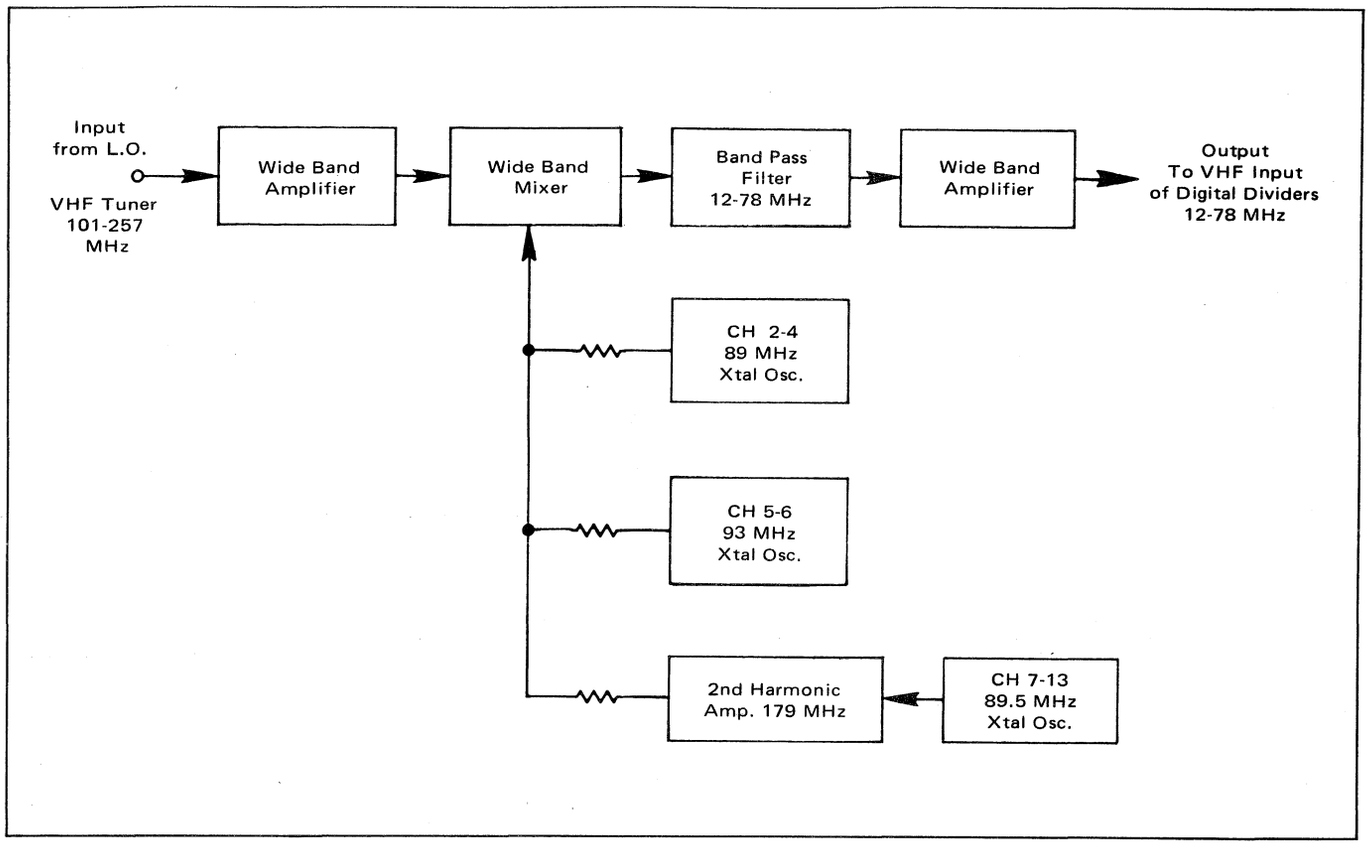


FIGURE 2 – VHF Local Oscillator Offset Circuit Block Diagram

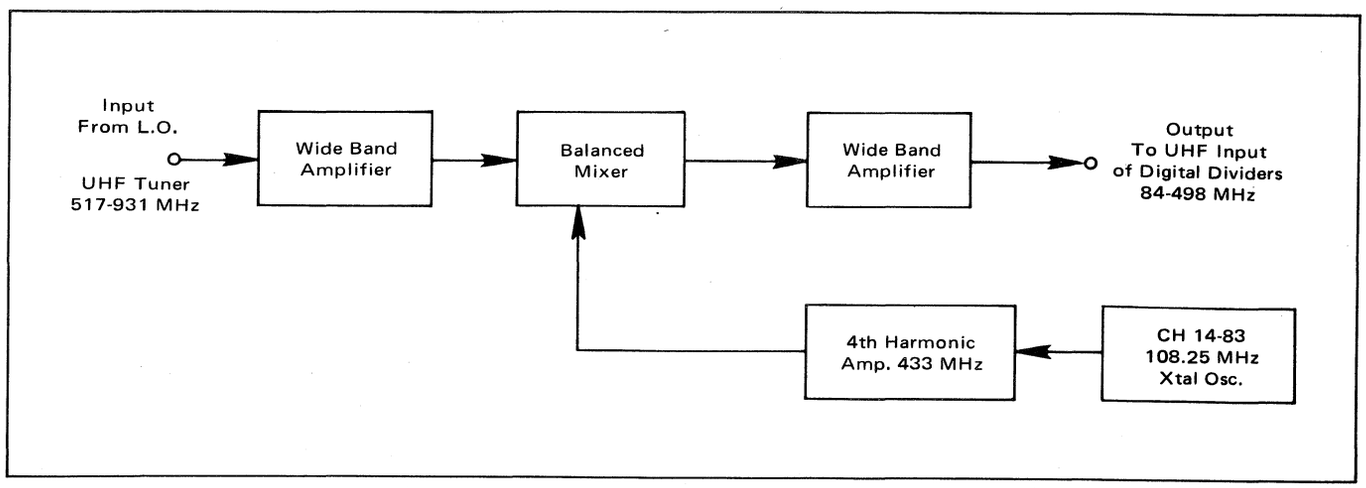


FIGURE 3 – UHF Local Oscillator Offset Circuit Block Diagram

between channel number and frequency, the following formula was used.

$$f_{os} = f_{lo} - N\,(CS)$$

Where: f_{os} = Frequency of the offset oscillator

f_{lo} = Frequency of the tuners' local oscillator at the desired channel number

N = The desired channel number

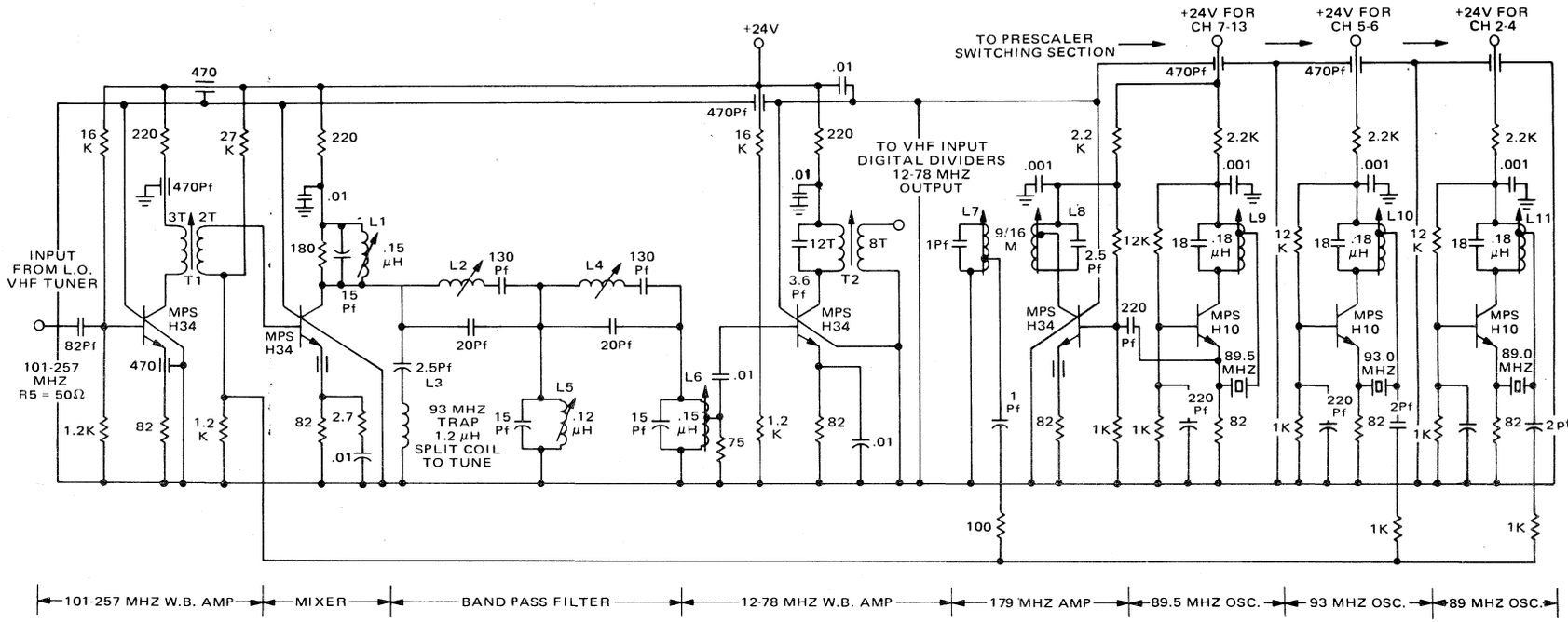
CS = Channel spacing (6 MHz)

See Table I for TV broadcast channels.

Figures 4 and 5 show the complete circuit diagrams of the VHF and UHF local oscillator offset circuits. The VHF tuner local oscillator output was approximately 30 mV when tuned to channel 2 and the UHF was approximately 10 mV across the whole band. It is essential that extreme care be taken with all circuit layout and shielding especially with the UHF local oscillator offset circuits.

TABLE 1 – OFFSET OSCILLATOR FREQUENCY CHART

	Channel (N)	f_{lo} Tuner Osc. Freq. (MHz)	f_{os} Offset Osc. Freq. (MHz)	Offset Osc. Sample Freq. (MHz)
Group I	2 ↓ 4	101 ↓ 113	89	12 ↓ 24
Group II	5 6	123 129	93	30 36
Group III	7 ↓ 13	221 ↓ 257	179	42 ↓ 78
Group IV	14 ↓ 83	517 ↓ 931	433	84 ↓ 498



T1
PRI. 3T
SEC. 2T
#26 T.N.A.
#10 COIL FORM
61 SLUG 1/2"

L1 & L6
20 1/2T #22
CLOSE WOUND
#10 COIL FORM
5-CORE 1/2"
TAP L6 14T FROM GROUND

L3
20T #30 T.N.A.
CLOSE WOUND
.2" I.D.
AIR CORE

L7 – L11
5-5T #22
SPACE WOUND
#10 COIL FORM
J-CORE 3/8"
TAP 1-3/4T

T2
PRI. 12T
SEC. 7T
#30 T.N.A.
1/4" COIL FORM
#61 SLUG 1/2"

L2 & L4
4-1/2T #22
SPACE WOUND
#10 COIL FORM
J-CORE 3/8"

L5
19-1/2T #22
CLOSE WOUND
#10 COIL FORM
E-CORE 1/2"

ALL COILS ARE IN COILCRAFT UNI-COIL KIT EXCEPT L3,
89 & 93 MHz XTALS ARE = ±0.01%
89.5 MHz XTAL IS = ±0.0025%

FIGURE 4 – VHF Offset Oscillators, Wide Band Mixer & Amplifier

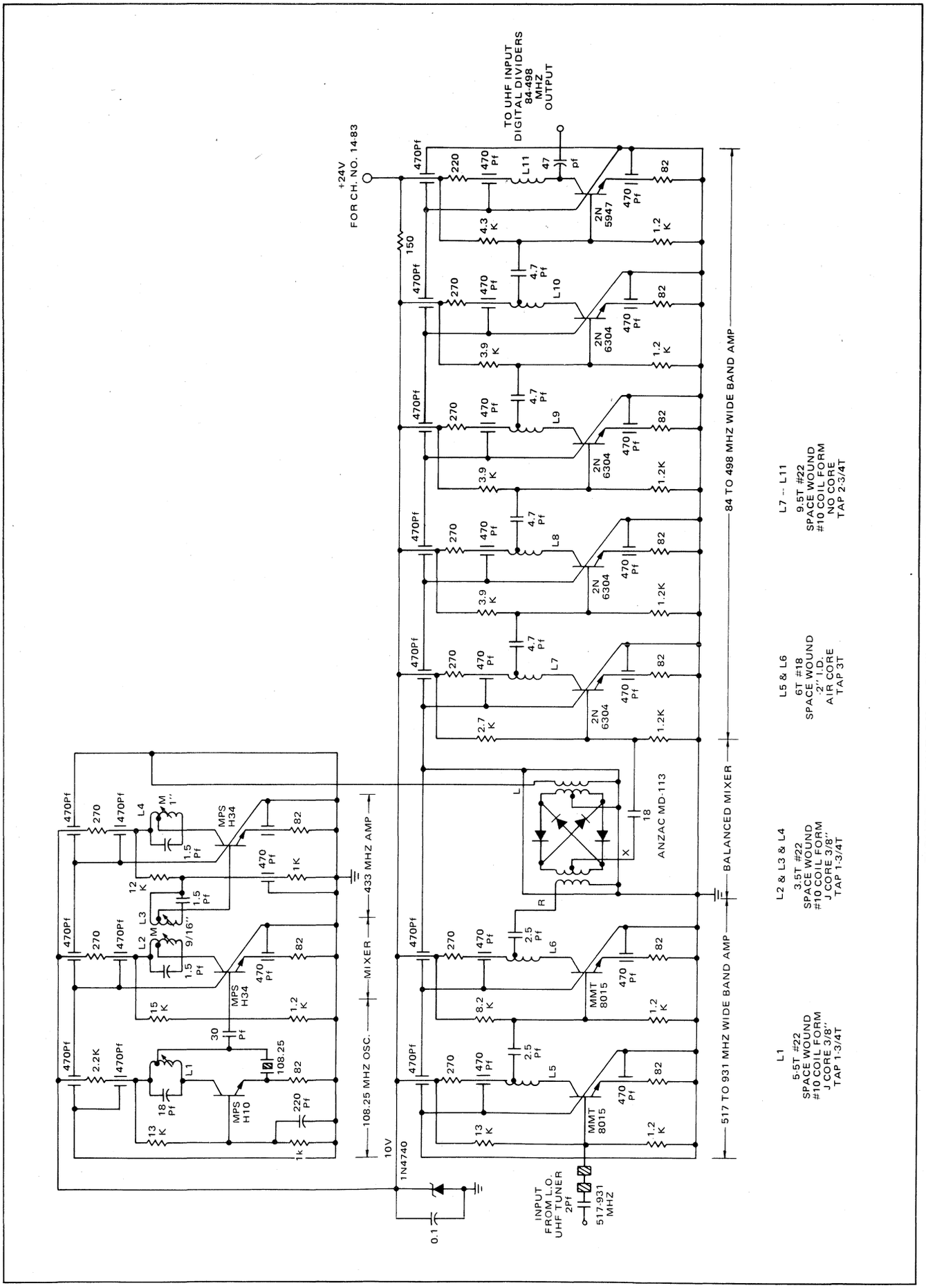


FIGURE 5 – UHF Offset Oscillator, Wide Band Mixer & Amplifier

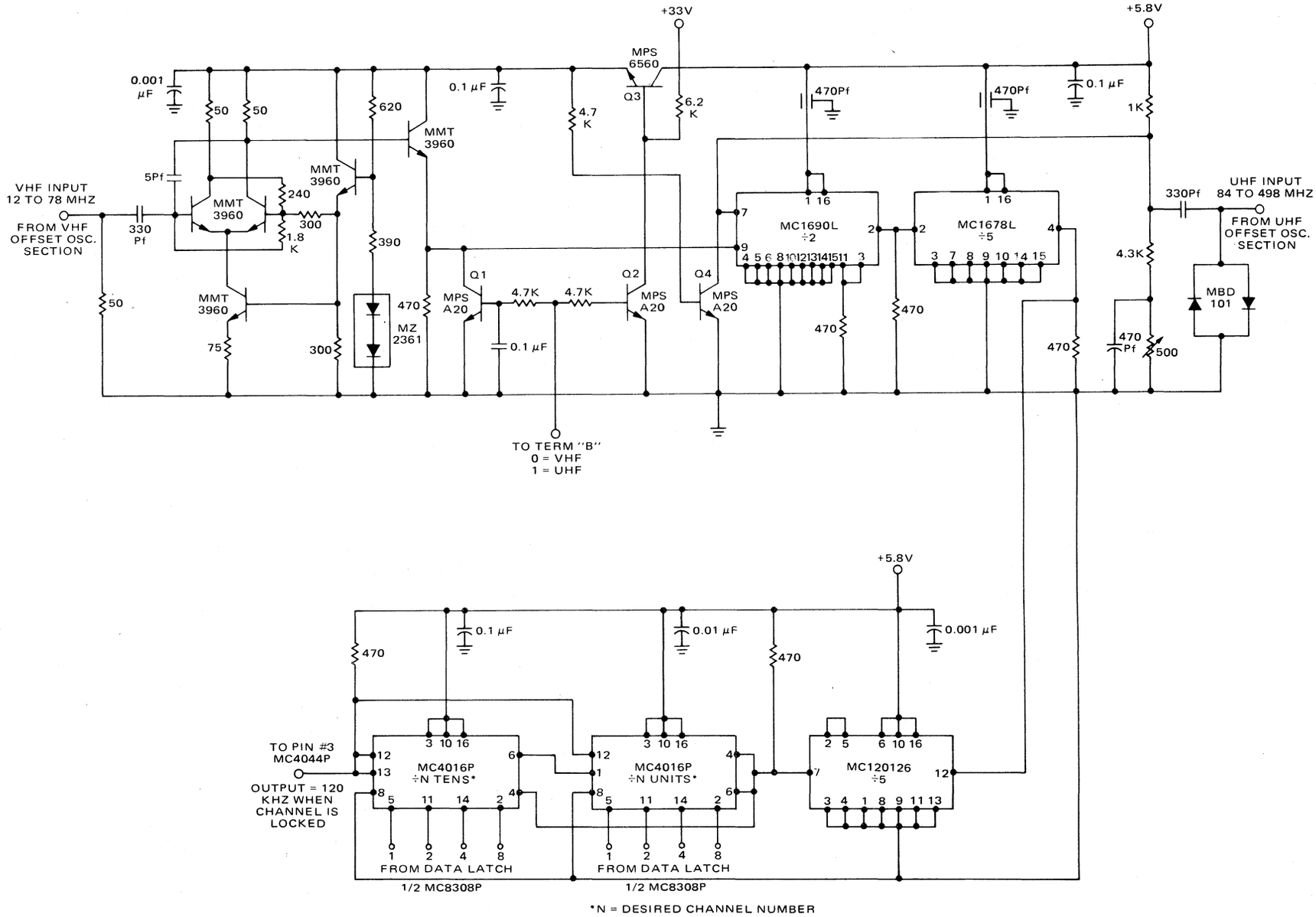


FIGURE 6 – Digital Dividers

DIGITAL DIVIDERS

A circuit diagram of the digital dividers is shown in Figure 6. The purpose of the digital dividers is to divide the offset local oscillator sample for comparison with the reference oscillator. A Schmitt Trigger, composed of five MMT3960s, is used on the VHF input to the MC1690L. The purpose of this circuit is to eliminate unwanted harmonics generated in the VHF wideband mixer which causes false triggering of the first divider. The harmonics show up in the form of amplitude modulation on the desired input signal. The UHF input is terminated with a pair of MBD101s which aids in peaking the high frequency harmonics of the input or squaring the sine waves by limiting the amplitude.

Transistors Q1 through Q4 perform the proper selection of either the VHF or UHF input depending on the channel number selected.

The first three dividers MC1690L, MC1678L, and MC12012L, are MECL high-speed, non-saturating logic which form a divide by 50. The number 50 was chosen so that the maximum divided input frequency would be in the range of standard TTL logic, 10 MHz or less. For channel 83 this gives a frequency of 9.96 MHz. Since the channel spacing is 6 MHz, and the prescaler divides by 50, the comparator reference must be 120 kHz, i.e., 6 MHz divided by 50. Two-cascaded MC4016Ps are used to divide by channel number thus giving a 120 kHz output when the correct oscillator frequency is obtained. Pull-up resistors, R1 and R2, are used to insure that the dividers will operate beyond 10 MHz.

PHASE-LOCKED LOOP SECTION

The purpose of the PLL section is to compare the offset and divided oscillator sample to the reference oscillator and correct the tuning voltage to obtain a frequency match. Figure 7 shows the PLL section which is made up of the reference oscillator, phase-frequency comparator and tuning voltage generator.

The output of the digital dividers is fed into the variable frequency input of the MC4044P phase-frequency comparator. The reference input is driven by the 120 kHz reference crystal oscillator with a squaring amplifier. The output error signal at point "a" will sit at 1.5 V when the loop is locked. The varactor-voltage generator consists of six-low cost transistors forming an inverting amplifier with an output voltage range from 0.8 to 31 V. The feedback loop C1 and R1 were chosen to overdamp the amplifier because of the limited overshoot range capability of the varactor tuner oscillators. The maximum loop lock-up time occurs when changing from channel 83 directly to 2 and is less than 250 ms. This looks instantaneous to the user.

Transistor Q5 saturates whenever any key is pressed which starts the tuning voltage at approximately 32 volts and always causes the loop to lock-up from the high frequency direction. This eliminates problems caused by the tuner local oscillators "misbehaving" if approximately 0 volts is applied to the tuning voltage line.

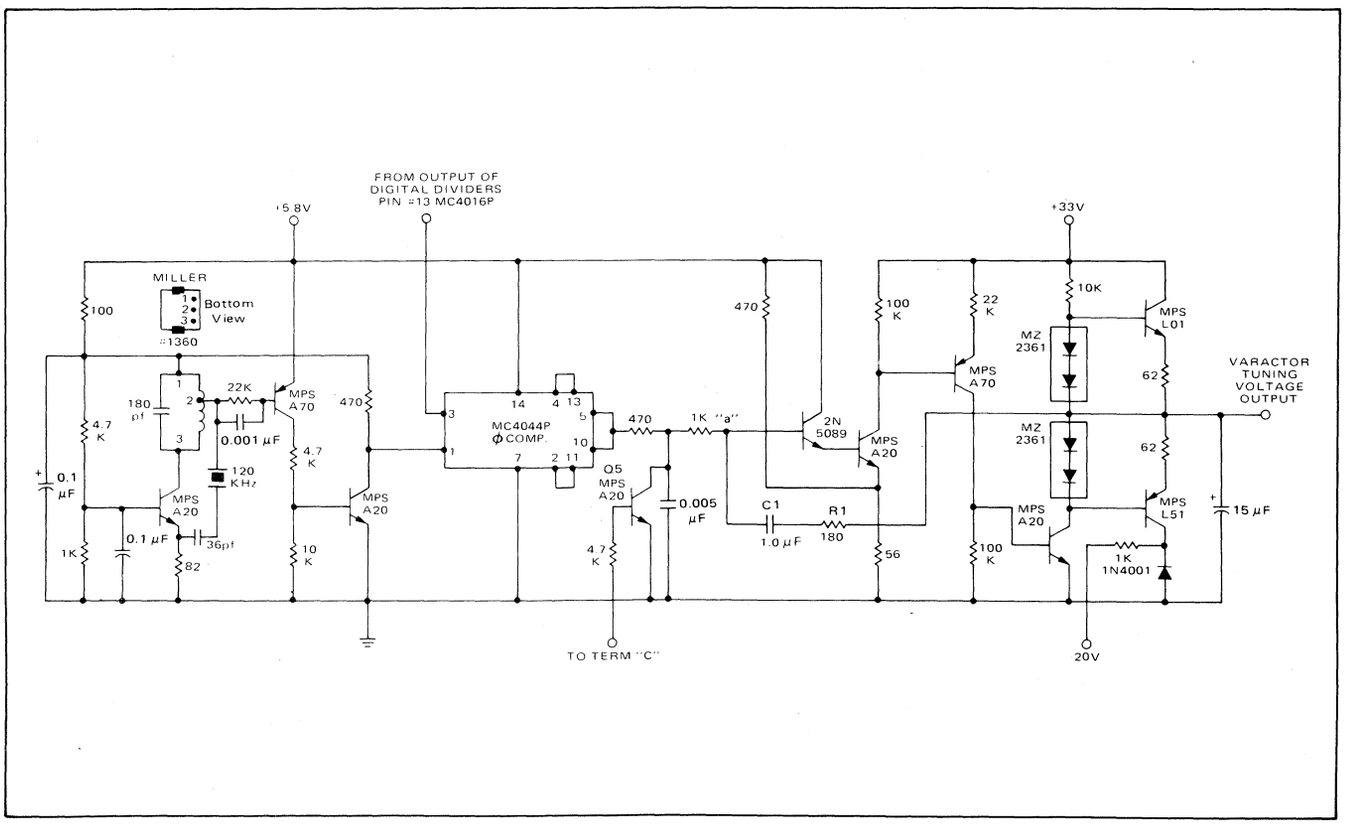


FIGURE 7 – Reference Oscillator, Phase-Frequency Comparator and Varactor-Voltage Generator

CUSTOMER INTERFACE

Figure 8 shows the customer interface which is made up of a keyboard address, data input steering network, memory, and seven-segment decoder/drivers. The purpose of the customer interface section is to accept channel number inputs from the user by means of a ten-button keyboard and pass this information in BCD form to the B+ control, the digital divider, and the readout circuits. The input from the keyboard is decoded to binary coded decimal by the use of fifteen diodes. Four extra diodes are used to provide a high state at terminal "C" whenever any key is pressed. This is used in conjunction with the data input steering network to change the serially-entered data to parallel form. The units and tens inputs of the data latch are tied together and data is entered into each section by bringing the master reset high and then the enable inputs of the appropriate section high. The units and tens output of the data latch drive the seven-segment decoders, tuning B+ controls, and the divide by "N" counters.

The MC8601P one-shot is used to clean leading edge contact bounce on the terminal "C" pulse before driving the MC7479P toggle flip-flop. The MC7479P drives two MC8602P dual one-shots which are wired 180° out of phase. The second section of the MC8602P is cascaded to the first, so that when toggled by the MC7479P it will first strobe the master reset and then the enable lines of either the tens or units section of the data latch.

This will, in turn, erase the previous data and store the new data before the key is released. Capacitor C2 and resistor R2 insure that pin 5 of the MC7479P will be low when the power is turned on. By doing this, the first number entered will go into the tens section of the data latch.

B+ CONTROL

The B+ control circuit diagram is shown in Figure 9. The purpose of the B+ control circuit is to look at the channel number selected, indicate an invalid channel number selection by flashing the number on the readout, provide B+ to the proper tuner, bandswitch, wideband amplifier, and offset oscillator, and provide sound mute and picture blanking outputs.

This circuit takes the two-digit BCD channel number and decodes the channel numbers into the four groups shown earlier in Table I, and an additional group which consists of invalid TV channel numbers. It then provides B+ to the proper circuits throughout the system according to the particular group into which the selected channel number falls. Figure 10 is marked so that the circuit operation can be followed easily and to aid in trouble-shooting.

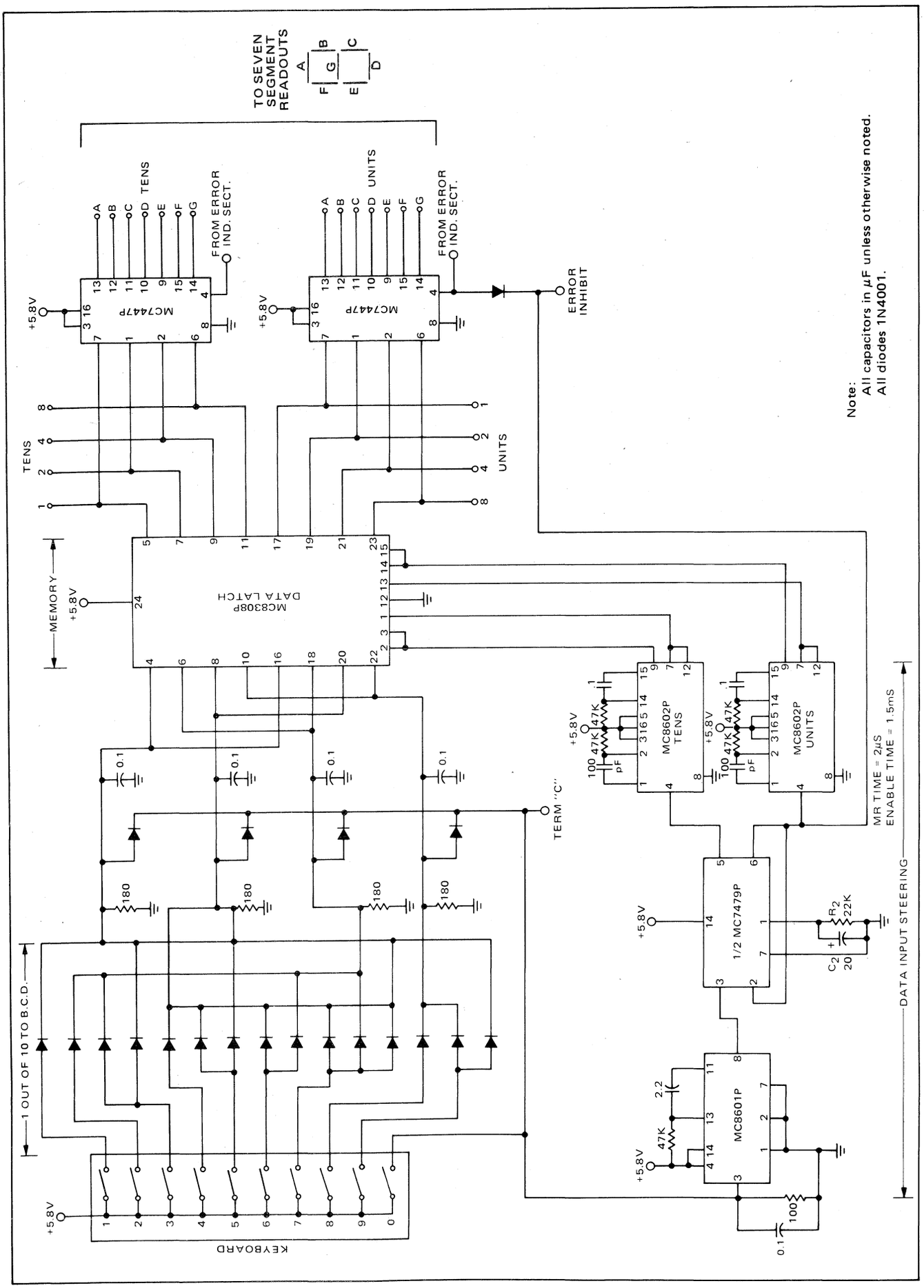


FIGURE 8 – Keyboard Address, Memory, and Seven Segment Driver

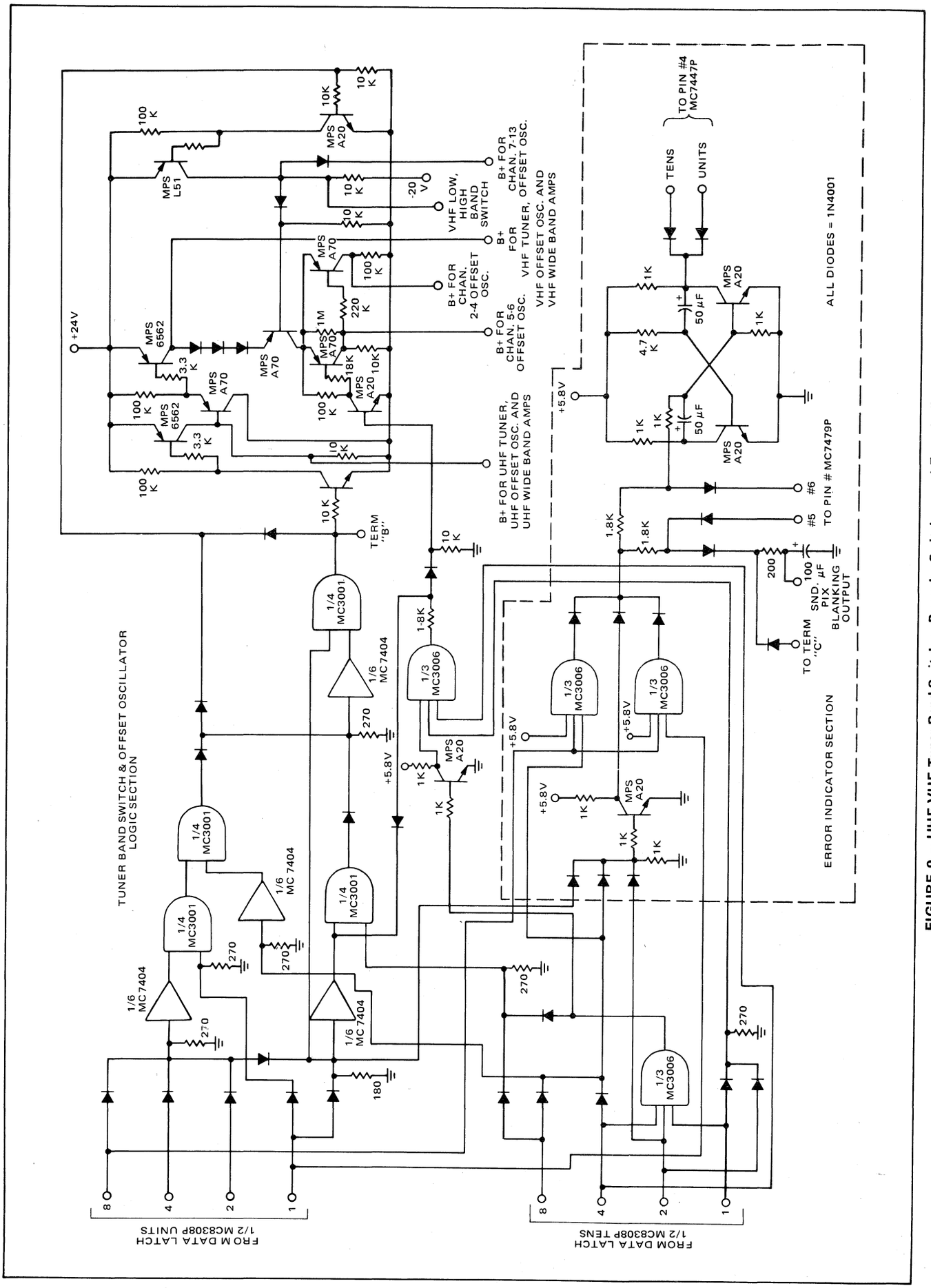


FIGURE 9 – UHF-VHF Tuner Band Switches, Prescaler Switches, and Error Indicator

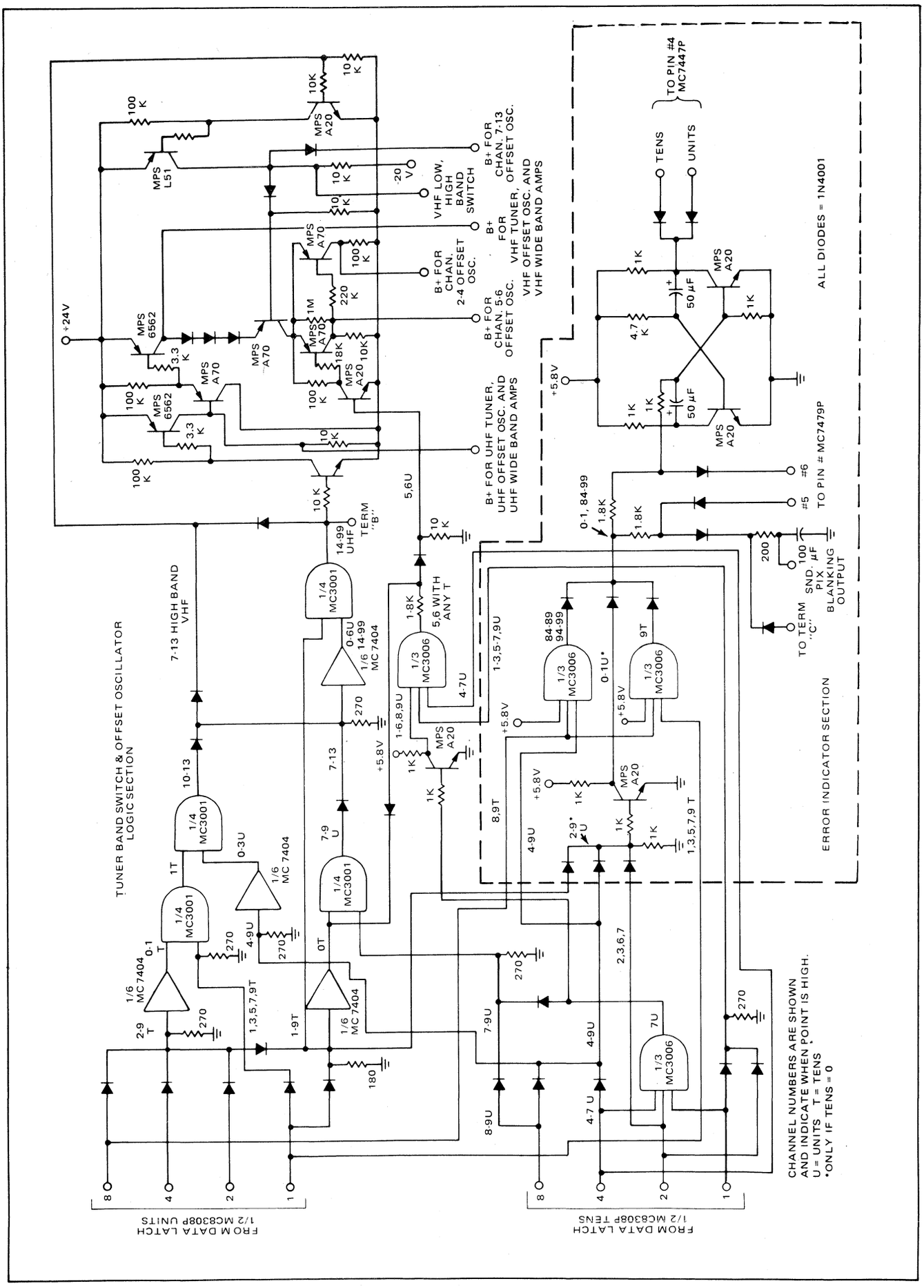


FIGURE 10 – UHF–VHF Tuner Band Switches, Prescaler Switches, and Error Indicator

POWER SUPPLY

Figure 11 shows the power supply used to generate the voltages necessary for the tuners and tuning system. Also shown in the figure are the maximum currents drawn from each of the supply voltages.

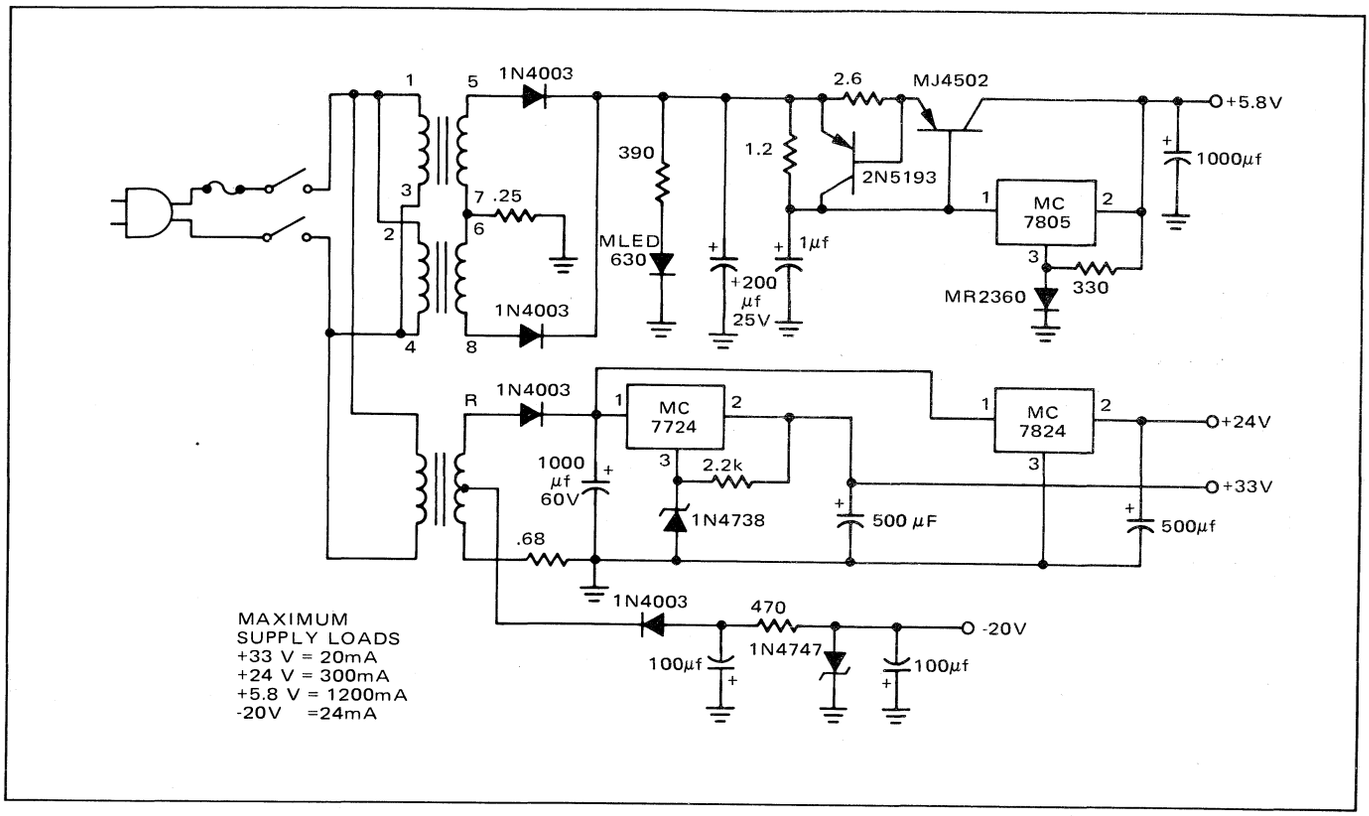


FIGURE 11 – Power Supply

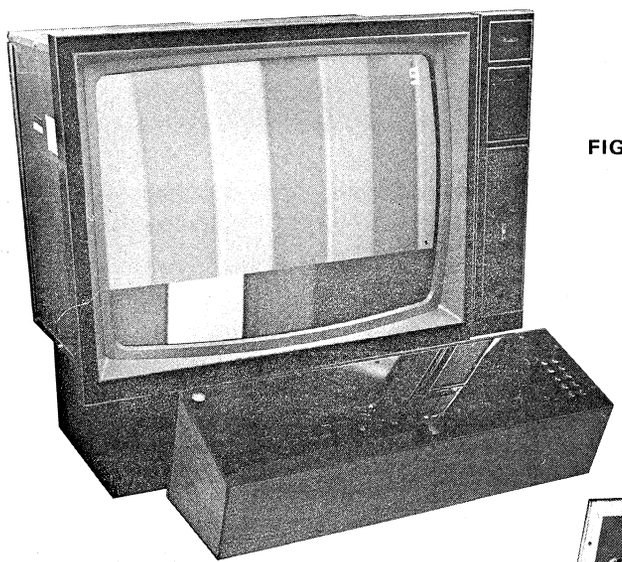
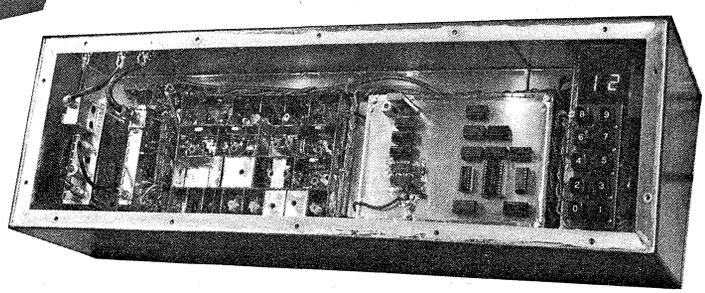


FIGURE 12

FIGURE 13



CONCLUSIONS

The system described here was constructed to show that off-the-shelf logic can be used to build a PLL tuning system for television using varactor tuners. The circuits, other than the ICs, are first time "go-arounds" and can undoubtedly be simplified. For example, tracking amplifiers could be used in place of the wideband amplifiers and wideband filters. This would also give more gain, thus requiring less stages. Also, the tuners could be designed with oscillator sample ports to deliver more energy to the tuning system without affecting tuner performance.

It is hoped that this presentation will provide adequate information to stimulate more designs for frequency domain control of varactor tuners.

The system was connected to a Heathkit GR2000 color television. Figures 12 and 13 show the completed system.

CREDITS

1. Many thanks to Heathkit for furnishing the television Model #GR2000.
2. The varactor tuners used were furnished by Zenith, Models 175-1503 VHF and 175-1604 UHF.
3. The push-button switches used were Clare #820.
4. The crystals were purchased from International Crystal Manufacturing Company.
5. Most of the coils used came from the Coilcraft Uni-coil Kit.

REFERENCES

1. Micro-T Packaged Transistors for High-Speed Logic Systems. Motorola Application Note AN-536, B. Broeker.
2. MECL System Design Handbook. Motorola Semiconductor Products, Inc., W. R. Blood, Jr.
3. Phase-Locked Loop Systems Data Book. Motorola Semiconductor Products, Inc.

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